**MOSCAP AC Characterization Report (Oxide Growth Time Variation)**

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**Device:** MOS Capacitor (MOSCAP)

**Measurement:** AC capacitance vs gate voltage (C–V) at temperatures from **300 K to 400 K**, for four devices fabricated with different oxide thicknesses.

**Figure:** Attached plot titled “AC characteristics.png” (C(g,g) vs Vg for multiple devices with different oxide growth times).

**Abstract**

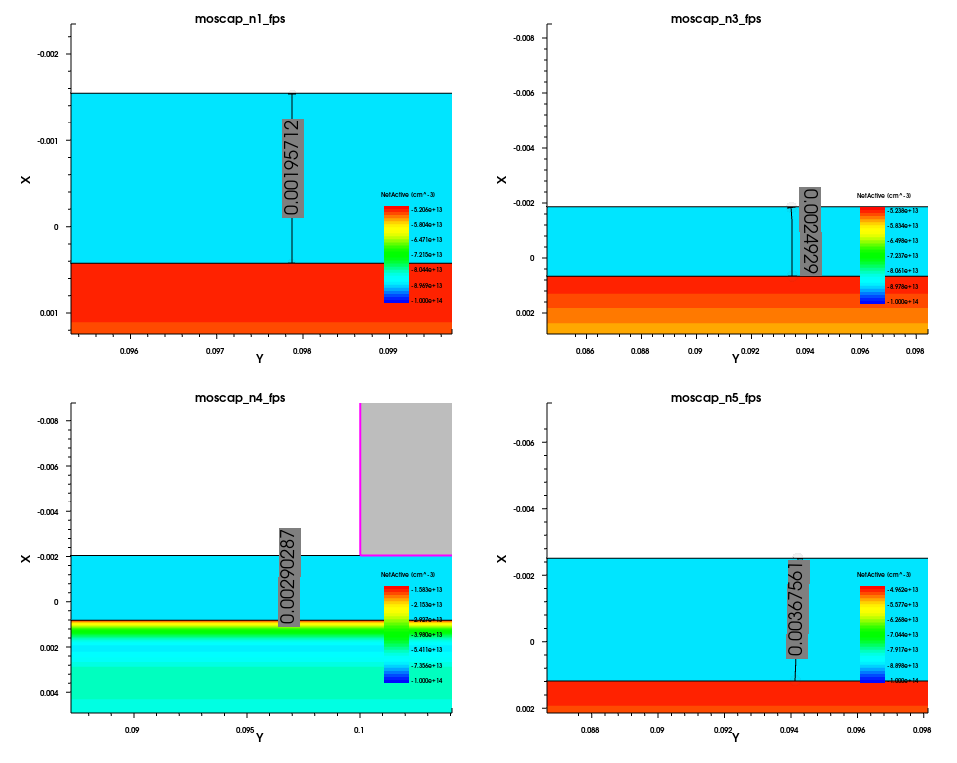
This report presents the AC C–V characterization of MOS capacitors simulated in Sentaurus TCAD. Four MOSCAPs were fabricated/simulated with different oxide thicknesses obtained by varying the **oxide growth time** during thermal oxidation. The AC capacitance was measured as a function of gate voltage over the temperature range 300 K–400 K. The aim is to investigate how varying oxide thickness influences the accumulation, depletion, and inversion capacitances, and to observe temperature-dependent variations in C–V characteristics.

**1. Device & Process Summary**

* **Structure:** Metal–oxide–semiconductor capacitor (MOSCAP)
* **Oxide:** Thermal SiO₂, grown under identical temperature but **different oxidation times**, resulting in different oxide thicknesses for each of the four devices.
* **Oxide thickness (t\_ox):** Varies with oxidation time; longer oxidation time yields thicker oxide and hence lower oxide capacitance (Cox ∝ 1/t\_ox).
* **Substrate:** p-type (or n-type) silicon with uniform doping concentration.
* **Gate electrode:** Ideal metal gate.
* **Process steps:** Implemented using sprocess — oxidation (time varied), implant/diffusion (for substrate doping), and metallization.

**2. Simulation Setup**

* **Tool:** Synopsys Sentaurus TCAD
* **Analysis type:** Small-signal AC (capacitance extraction)
* **Parameter sweep:** Gate voltage (Vg) swept from –3 V to +3 V
* **Temperature range:** 300 K – 400 K
* **AC frequency:** (To be provided; typically 1 MHz or 100 kHz)
* **Variation:** Oxide thickness controlled via oxidation time (4 different values)
* **Bias conditions:** Gate voltage swept; substrate grounded.



The above plot shows the variation in oxide thickness when the diffusion time is varied.

SPROCESS code for structure generation-

math coord.ucs  
line x location= 0.0 spacing= 1.0<nm> tag= SiTop  
line x location= 50.0<nm> spacing= 1.0<nm>  
line x location= 0.5<um> spacing= 50.0<nm> tag= SiBottom  
line y location= 0.0 spacing= 1.0<nm> tag= Mid  
line y location= 0.40<um> spacing= 1.0<nm> tag= Right  
region Silicon xlo= SiTop xhi= SiBottom ylo= Mid yhi= Right  
init concentration= 1e14<cm-3> field= Boron  
AdvancedCalibration  
pdbSet Grid NativeLayerThickness 1e-7  
pdbSet Oxide Grid perp.add.dist 1e-7  
diffuse temperature= 850<C> time= @time\_o@<min> O2  
deposit material= {Aluminum} type= isotropic time= 1 rate= {0.03}  
mask name= contacts\_mask left= 0.1<um> right= 0.3<um>  
etch material= {Aluminum} type= anisotropic time= 1 rate= {0.25} mask= contacts\_mask  
contact name="body" bottom Silicon  
contact name="gate" box Aluminum xlo=-0.04 xhi=0 ylo= 0 yhi= 0.4  
struct tdr = moscap\_n@node@  
exit

To receive the capacitance plot we have to enter the following code in sdevice-

# Temperature Range: 300 K – 400 K (to be varied externally)

###############################################################

Device "MOS" {

###########################################################

# 1. File and Output Setup

###########################################################

File {

Grid = "moscap\_fps.tdr" # Mesh structure file from sprocess

Plot = "moscap\_N" # Output plot prefix

Parameter= "moscap\_N" # Optional parameter set name

Current = "moscap" # Current data output

}

###########################################################

# 2. Electrical Contacts (Electrodes)

###########################################################

Electrode {

{ Name = "gate" Voltage = 0.0 }

{ Name = "body" Voltage = 0.0 }

}

###########################################################

# 3. Physical Models

###########################################################

Physics {

Fermi # Enables Fermi–Dirac statistics

EffectiveIntrinsicDensity( OldSlotboom ) # Improved carrier statistics

Mobility( # Carrier mobility models

DopingDep # Doping-dependent mobility

eHighFieldsaturation( GradQuasiFermi ) # Electron high-field saturation

hHighFieldsaturation( GradQuasiFermi ) # Hole high-field saturation

Enormal # Normal electric field dependence

)

Recombination( # Carrier recombination models

SRH( DopingDep TempDependence ) # Shockley–Read–Hall with T dependence

)

}

###########################################################

# 4. Quantities to be Plotted (Results to extract)

###########################################################

Plot {

# Carrier densities and currents

eDensity hDensity

TotalCurrent/Vector eCurrent/Vector hCurrent/Vector

eMobility hMobility

eVelocity hVelocity

eQuasiFermi hQuasiFermi

# Temperature fields

eTemperature Temperature hTemperature

# Electric fields and potential

ElectricField/Vector Potential SpaceCharge

# Doping information

Doping DonorConcentration AcceptorConcentration

# Recombination and generation

SRH Band2BandGeneration Auger

ImpactIonization eImpactIonization hImpactIonization

# Driving forces

eGradQuasiFermi/Vector hGradQuasiFermi/Vector

eEparallel hEparallel eENormal hENormal

# Band structure information

BandGap BandGapNarrowing Affinity

ConductionBand ValenceBand eQuantumPotential

}

###########################################################

# 5. Numerical Solver Settings

###########################################################

Math {

RelErrControl

Digits = 5

ErrRef(electron) = 1.e10

ErrRef(hole) = 1.e10

Iterations = 20

Notdamped = 100

Method = Blocked

SubMethod = Super

ACMethod = Blocked

ACSubMethod = Super

}

###########################################################

# 6. Output File Names

###########################################################

File {

Output = "moscap@node@" # DC and AC data output prefix

ACExtract = "moscap@node@" # AC extraction results

}

###########################################################

# 7. Circuit Connections (System Definition)

###########################################################

System {

# Physical device instance

MOS nmos1 ( "body" = b "gate" = g )

# External voltage sources

Vsource\_pset vb (b 0) { dc = 0.0 } # Body bias (grounded)

Vsource\_pset vg (g 0) { dc = 0.0 } # Gate bias (swept)

}

###########################################################

# 8. Solution Sequence

###########################################################

Solve {

# Step 1 — Initial potential solution

NewCurrentPrefix = "init\_"

Coupled(Iterations = 100) { Poisson }

# Step 2 — Equilibrium (DC bias)

Coupled { Poisson Electron Hole }

# Step 3 — DC sweep (Vg from 0 → -3 V)

Quasistationary (

InitialStep = 0.1

Increment = 1.3

MaxStep = 0.5

MinStep = 1.e-5

Goal { Parameter = vg.dc Voltage = -3.0 }

) {

Coupled { Poisson Electron Hole }

}

# Step 4 — AC Analysis (Vg from -3 V → +3 V)

NewCurrentPrefix = ""

Quasistationary (

InitialStep = 0.01

Increment = 1.3

MaxStep = 0.05

MinStep = 1.e-5

Goal { Parameter = vg.dc Voltage = 3.0 }

) {

ACCoupled (

StartFrequency = 1E6 # 1 MHz AC frequency

EndFrequency = 1E6

NumberOfPoints = 1

Decade

Node(g b) # Capacitance between gate and body

Exclude(vg vb)

ACCompute (Time = (Range = (0 1) Intervals = 40))

) {

Poisson Electron Hole

}

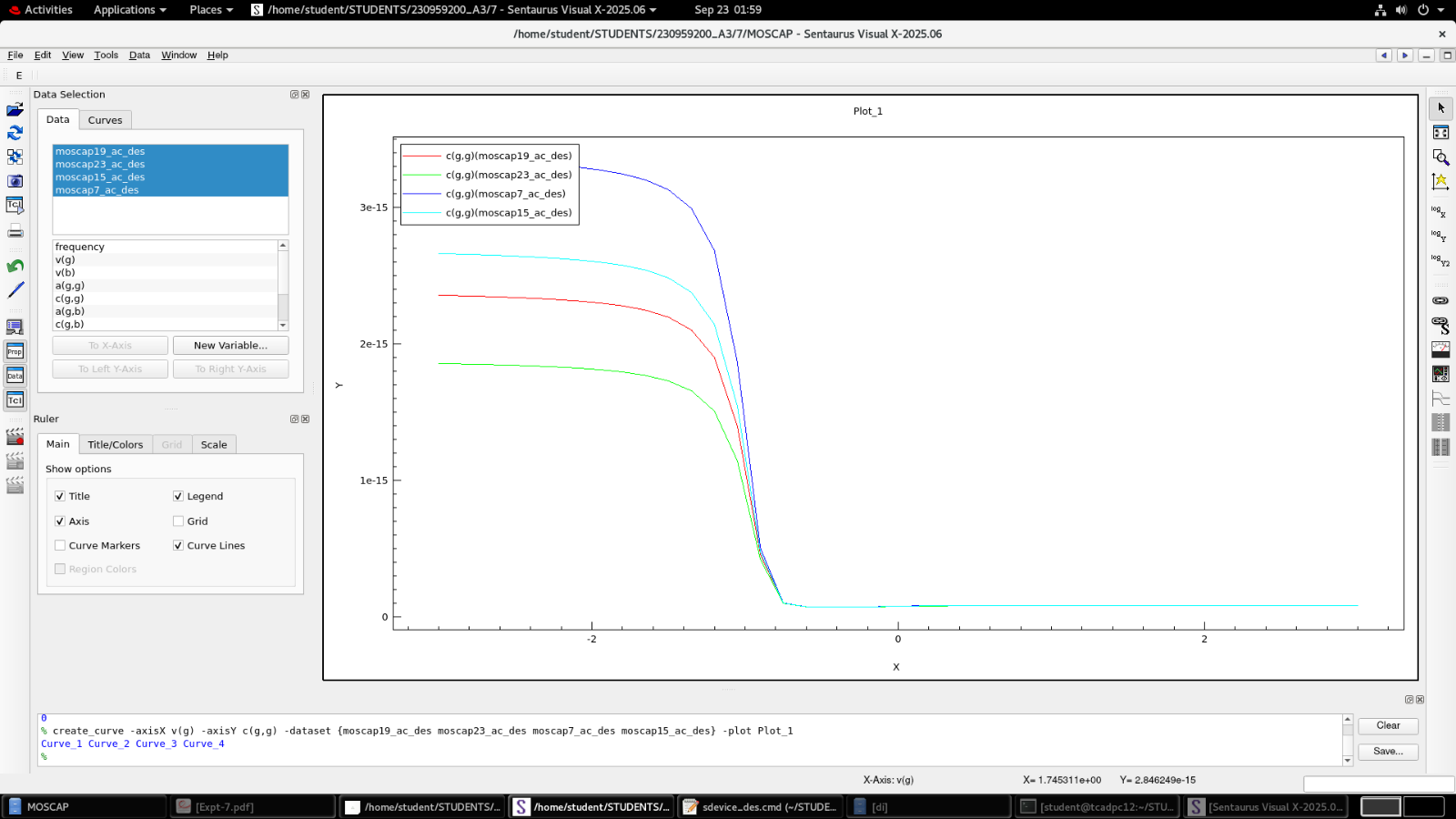
}

}

}

###############################################################

# End of File

Output plot-

**Interpretation**

* **Oxide thickness effect:** The vertical separation of C–V curves corresponds to the expected difference in oxide capacitance values caused by different oxidation times.
* **Temperature effect:** Minor lateral or vertical shifts may arise from semiconductor intrinsic property changes with temperature.
* **Frequency consideration:** At high AC frequencies, inversion capacitance remains low; if low-frequency data is used, inversion capacitance can increase due to minority carrier response.

**Conclusions-**

* Varying oxidation time successfully produced MOS capacitors with different oxide thicknesses, confirmed through varying accumulation capacitance values.
* The accumulation capacitance decreases as oxide thickness increases (C ∝ 1/t\_ox).
* Temperature variation between 300–400 K introduces small but noticeable changes in C–V characteristics, mainly due to intrinsic carrier and bandgap effects.
* The simulation agrees with theoretical expectations for MOS capacitors with varying oxide thickness.